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Effective on 12/08/2004.
Fees Pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/372,879
Filing Date	August 12, 1999
First Named Inventor	Sidiropoulos
Examiner Name	Farahani, D.
Art Unit	2891
Attorney Docket No.	RAMB-01014US0

METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): Vierra Magen Marcus

☑ Deposit Account Deposit Account Number: Harmon & DeNiro LLP Deposit Account Name: 501826

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____ x	50 =	0

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____ x	200 =	0

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims: Fee ($) _____ Fee Paid ($) _____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number) x	_____ =	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Appeal Brief	500

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 35,854	Telephone 415-369-9660
Name (Print/Type)	Kirk J. DeNiro	7/5/05	Date July 5, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application		PATENT APPLICATION
Inventors:	Stefanos Sidiropoulos, et al.	
Application No.:	09/372,879	Art Unit: 2814
Filed:	Aug. 12, 1999	Examiner: Farahani, Dana
Title:	INTEGRATED CIRCUIT DEVICE HAVING I/O STRUCTURES WITH REDUCED INPUT LOSS	Customer No. 38456

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail in an envelope addressed to **Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**, on July 5, 2005.

7/5/05

Kirk J. DeNiro, Reg. No. 35,854
Signature/Date: July 5, 2005

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This APPEAL BRIEF is submitted in accordance with 37 C.F.R. §1.192, in triplicate, following the NOTICE OF APPEAL filed by Appellant on May 4, 2005. The fee set forth in 1.17(c) is submitted herewith.

07/11/2005 MBERHE 00000021 09372879
01 FC:1402 500.00 OP

Attorney Docket No.: RAMB-01014US0
ramb/1014/1014.appeal brief

Table of Contents

I. REAL PARTY IN INTEREST (37 C.F.R. §1.192(c)(1))

The real party in interest is Rambus Inc.

II. RELATED APPEALS AND INTERFERENCES *(37 C.F.R. §1.192(c)(2))*

Appellant knows of no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending Appeal.

III. STATUS OF CLAIMS *(37 C.F.R. §1.192(c)(3))*

Claims 1-24 and 26-45 are pending in Patent Application No. 09/618,955 (herein "Application"). Claims 1-12 have been allowed. Claims 12-24 and 26-45 stand finally rejected. Appellant herein appeals from the final rejection of each of claims 12-22.

IV. STATUS OF AMENDMENTS *(37 C.F.R. §1.192(c)(4))*

Concurrently filed with this APPEAL BRIEF is an amendment after final rejection under 37 C.F.R. § 1.116 in order to present the rejected claims in better form for Appeal. An amendment after final rejection was submitted on March 30, 2005 that cancelled claims 23-27 on the belief that claims 1-22 were allowed as indicated in the Office Action dated January 4, 2005 (herein "Office Action") and a conversation with the Examiner on March 29, 2005. However, an Advisory Action mailed April 12, 2005 indicated that the previously submitted amendment after final did not place the Application in condition for allowance because: "claims 1-11 were meant to be allowed in the Last Office Action, and not claims 1-22. Citing claims 1-22 as the allowed claim was a typographical error." Accordingly, the Examiner is respectfully requested to enter the concurrently filed amendment after final rejection for the purpose of this Appeal.

V. SUMMARY *(37 C.F.R. §1.192(c)(5))*

Embodiments of the invention include a bond pad structure of an integrated circuit device, for example a memory device, which provides an increased operating frequency and range of the integrated circuit device. (Application, p. 9, lns. 2-5, pp. 14-15; Fig. 4B, "bonding pad 500"). In an embodiment, a bond pad structure includes a conductive bonding layer which is illustrated in Fig. 4B of the Application and provided below. (Fig. 4B, "conductive bonding layer

510" Application, p. 14, ln. 18). A doped region of a first conductive type is formed in a semiconductor substrate of a second conductive type. (Fig. 4B; "doped region 520" Application, p. 15, lns. 4-5). The doped region is underlying and surrounding the conductive bonding layer. A conductive region of the first conductivity type is disposed in the doped region. (Fig. 4; "conductive region 530" Application, p. 15, lns. 4-5). The conductive region is underlying and surrounding the conductive bonding layer. The conductive region includes a surface area at least substantially equal to a surface area of the conductive bonding layer. (Application, p. 15, lns. 7-9). A conductive tap region is spaced apart and surrounding at least a portion of the doped region. (Fig. 4B; "tap region 540" Application, p. 14, ln. 20). A portion of the conductive tap region is electrically coupled to a voltage supply. (Fig. 4B; "supply voltage 595" Application, p. 16, lns. 1-4).

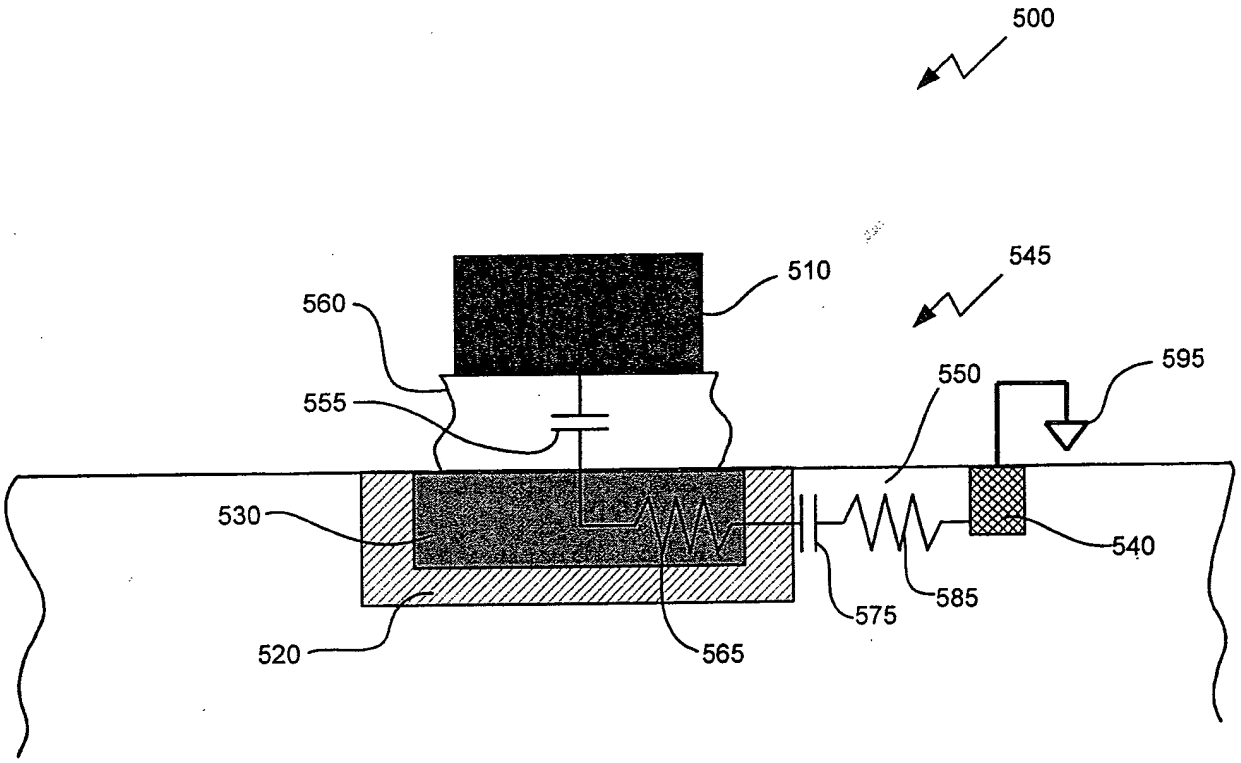


FIGURE 4B

VI. ISSUE *(37 C.F.R. §1.192(c)(6))*

Whether claims 12-22 of the Application are properly rejected under 35 U.S.C. §103 over U. S. Patent No. 6,329,694 B1 to Lee et al. (herein "*Lee et al.*").

VII. GROUPING OF CLAIMS *(37 C.F.R. §1.192(c)(7))*

Applicant requests for the purpose of review that claims 12-22 be grouped together.

VIII. ARGUMENT *(37 C.F.R. §1.192(c)(8))*

A. The *Lee et al.* Reference

Lee et al. describes "a semiconductor device with an electrostatic discharge (ESD) protection circuit..." (Abstract). *Lee et al.* describes an ESD circuit to dissipate current caused by electrostatic discharge that may damage internal circuits. (Col. 1, lns. 35, 52). *Lee et al.* describes embodiments of an ESD circuit that include NMOS and PMOS transistors having n-well/n+ guard rings or p+ guard rings. Figs. 3-4, 8A-8H and 9A-9H illustrate the various embodiments. As illustrated by Fig. 9D below, *Lee et al.* describes an ESD circuit including NMOS and PMOS transistors with a p+ guard ring. As can be seen, *Lee et al.* describes an ESD circuit that is clearly separate and different from a "DATA INPUT PAD" and an "INTERNAL CIRCUIT."

FIG. 9D

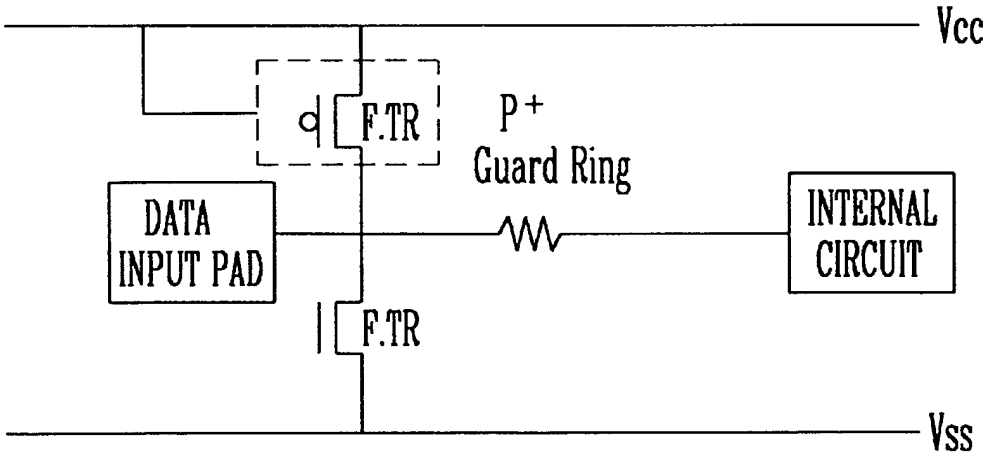
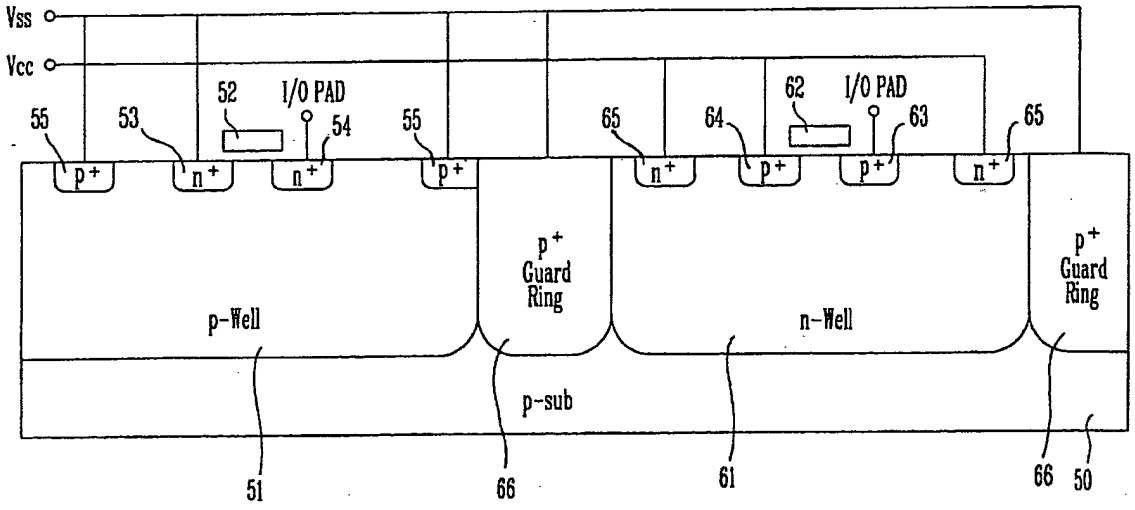


Fig. 14 shown below is a sectional view of the ESD protection circuit that includes the NMOS transistor and PMOS transistor having a p+ guard ring formed on a substrate 50. (Col. 4, ln. 39; Col. 5, lns. 35-59). As shown in Fig. 14, the ESD circuit is coupled to an "I/O PAD." The NMOS transistor is formed by a first gate electrode 52, a first source 53, a first drain 54 and a p+ pick-up 55 formed in p-well 51. The PMOS transistor is formed by a second gate electrode 62, a second source 63, a second drain 64 and a p+ pick-up 65 formed in n-well 61. The p+ guard ring 66 is "formed either connected to the p-well 51 and the n-well 61, or is formed isolated from the p-well 51." (Col. 5, lns. 57-59).

FIG. 14



B. <u>The Examiner Erred in Rejecting Claims 12-22 under 35 U.S.C. § 103 over *Lee et al.*</u>

1. <u>Claim 12 includes a limitation that the Examiner has already indicated is the basis for allowance over *Lee et al.*</u>

In the Office Action that allowed claims 1-11, the Examiner stated:

The primary reason for indication of allowability of the above noted claims is the inclusion therein of the limitation that of <u>a conductive region</u>

underlying and surrounding the conductive pad. This limitation is neither disclosed nor thought by the prior art of record. (Emphasis added).

Claim 12 calls for "the bond pad comprising: a conductive bonding layer"..."the conductive region is underlying and surrounding the conductive bonding layer..." The Examiner has not clearly stated how the cited references teach or suggest "a conductive bonding layer" of claim 12 , but not "a conductive pad" of allowed claim 1.

Therefore, claim 12 and dependent claims 13-22 should be allowable for at least the reasons stated by the Examiner in allowing claim 1.

2. *Lee et al.'s* ESD circuit is not a "bond pad" as stated in claim 12

In rejecting claim 12, the Examiner stated:

> Lee discloses the bond pad comprising conductive bonding layers 63-65; a first doped region 61 of the first conductivity type formed in a semiconductor substrate 50 of the second conductivity type, underlying and surrounding the conductive bonding layer; a conductive region 65 of the first conductivity type disposed in the first doped region underlying and surrounding the bonding layer 63, the conductive region having a surface area; and a conductive tap region 66 spaced apart from and surrounding at least a portion of the first doped region, wherein a portion of the conductive tap region is electrically coupled to a supply voltage. (Office Action, p. 2-3). (Emphasis added).

Lee et al. discloses an ESD circuit, as illustrated in Figs. 9D and 14, which is coupled to a "DATA INPUT PAD" or an "I/O PAD." *Lee et al.* clearly teaches that the ESD circuit shown in Figs. 9D and 14 is different and separate from the "bond bad" as in claim 12. An ESD circuit and a bond pad generally perform two separate functions. The purpose of *Lee et al.*'s ESD circuit is to dissipate current caused by electrostatic discharge that may damage internal circuits. (Col. 1, lns. 35, 52). In contrast, embodiments of the "bond pad" in claim 12 allow for "increased operating frequency and range to [a] device... coupled to a high speed bus..." (Application, p. 9, lns. 3-5).

Likewise, second source 64, second drain 63 and p+ pick-up 65 are not "a conductive bonding layer," but components of a PMOS transistor used in an ESD circuit.

3. **The Examiner is improperly using the same component disclosed in *Lee et al.* for two separate elements of claim 12**

Even assuming that the ESD circuit can be interpreted as the "bond pad" of claim 12, the Examiner is using p+ pick-up 65 shown in Fig. 14 as both the "conductive bonding layer" and "a conductive region" of claim 12.

Also, claim 12 calls for "a conductive bonding layer" and not "conductive bonding layers" (emphasis added) as stated by the Examiner.

Further, claim 12 calls for "...the conductive region is underlying and surrounding the conductive bonding layer..." [P]+ pick-up 65 is not "underlying and surrounding" second source 63, second drain 64 and p+ pick-up 65.

The Examiner stated in the Office Action:

> Lee does not disclose the surface region 65 substantially equal to the surface area of the conductive bonding layer. Note that by enlarging region 65 in order to equalize it with the conductive bonding region [*sic* layer], region 65 would have to be enlarged to the extent that it would have [*sic* to] make a direct connection to 64. since [*sic* Since] 64 and 65 are shorted together, the direct connection would have been another method to short these 64 and 65 together. Lee discloses at column 3, lines 8-12, that instead of metal strapping, the shortening [*sic* shorting] of the layers can be carried out by using semiconductor material. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to equalize 65 to the conductive bonding layer. A mere change in the size of a component is generally recognized as being within the level of ordinary skill in the art. See In re Rose, 105 USPQ 237 (CCPA 1955). (Office Action, p. 3).

Appellant's attorney respectfully disagrees. First, the Examiner is using p+ pick-up 65 for both a part of the "conductive bonding layers" and the "conductive region." Therefore, any alleged obvious enlargement of p+ pick-up 65 would also enlarge the conductive bonding layer that includes, according to the Examiner, p+ pick-up 65, second source 63 and second drain 64.

Second, while *Lee et al.* may disclose "shortening [*sic* shorting] the layers...by using semiconductor material," there is no teaching or suggestion that this shorting is done so "a surface area [of the conductive region is] at least substantially equal to a surface area of the conductive bonding layer..." There is no disclosure or suggestion of enlarging p+ pick-up

65. The Examiner is improperly using the present Application as a road map to pick and size components of *Lee et al.* "This form of hindsight reasoning, using the invention to find its prior art components, would discount the value of combining various existing features or principles in a new way to achieve a new result—often the very definition of invention." *Ruiz v. A.B. Chance Co.*, 357 F.3d 1270, 69 USPQ2d 1686 (Fed. Cir. 2004). One of ordinary skill in the art could create this shorting by numerous physical orientations other than the enlarging described by the Examiner. For example, p+ pick-up 65 could be positioned next to second drain 64 in order to cause the shorting without any enlarging. Likewise, the Examiner has not stated why one of ordinary skill in the art would be motivated to enlarge p+ pick-up 65 rather than second drain 64 and/or second source 63 to cause this shorting. The Examiner is using a vague disclosure of shorting in *Lee et al.* that does not describe shorting so "a surface area [of the conductive region is]at least substantially equal to a surface area of the conductive bonding layer..."

Third, the alleged obvious enlargement of p+ pick-up 65 is <u>not</u> "a mere change in the size of a component..." Enlarging p+ pick-up 65 would alter the voltage and current characteristics of the ESD circuit. An amount of enlarging p+ pick-up 65 may even cause the ESD circuit to become ineffective or inoperable.

IX. CONCLUSION

Based on the above, it is respectfully submitted that claims 12-22 are patentable over *Lee et al.*, and it is respectfully requested that the rejection of claims 12-22 under 35 U.S.C. § 103 over *Lee et al.* be withdrawn.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this Appeal Brief, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: July 5, 2005

By: _____
Kirk J. DeNiro
Reg. No. 35,854

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APPENDIX
CLAIMS ON APPEAL
37 C.F.R. §1.192(c)(9)[1]

1. (previously presented) An integrated circuit device comprising:

a bond pad structure including:

a conductive pad;

a first doped region of a first conductivity type disposed in a semiconductor substrate of a second conductivity type, wherein the first doped region is underlying and surrounding the conductive pad;

a conductive region of the first conductivity type, underlying and surrounding the conductive pad, disposed in the first doped region;

a first tap region spaced apart from and surrounding a substantial portion of the first doped region, wherein the first tap region is electrically coupled to a first supply voltage;

an output driver transistor having a drain region and a source region, wherein the drain region is electrically coupled to the conductive pad; and

a second tap region surrounding the output driver transistor, wherein the second tap region is electrically and physically coupled to a second supply voltage and the source region.

2. (previously presented) The integrated circuit device of claim 1 wherein the conductive pad includes a metal.

3. (previously presented) The integrated circuit device of claim 1 wherein the first tap region completely surrounds the first doped region, and wherein the first and second supply voltages are ground.

4. (previously presented) The integrated circuit device of claim 1 wherein the first tap region is a discontinuous region.

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[1] Claims 12 and 15 includes amendments in a concurrently filed amendment after final rejection under 37 C.F.R. § 1.116. Likewise, claims 38-45 have been concurrently cancelled.

5. (previously presented) The integrated circuit device of claim 1 wherein a doping concentration of the first doped region is less than a doping concentration of the conductive region.

6. (previously presented) The integrated circuit device of claim 1 wherein the first tap region is a second doped region and the second tap region is a third doped region.

7. (previously presented) The integrated circuit device of claim 6 wherein the second doped region is of an opposite conductivity type than the first doped region.

8. (previously presented) The integrated circuit device of claim 6 wherein the third doped region is a P type doped region and the output driver transistor is an NMOS type transistor.

9. (previously presented) The integrated circuit device of claim 1 further including a tap region portion that is spaced apart from and surrounding the first doped region, wherein the tap region portion is decoupled from the first supply voltage to provide a predetermined resistance between the first doped region and the first supply voltage.

10. (previously presented) The integrated circuit device of claim 1 wherein a portion of the second tap region is integrated into the source region.

11. (previously presented) The integrated circuit device of claim 10 wherein the first tap region is a discontinuous region.

12. (previously presented) A bond pad for an integrated circuit device, the bond pad comprising:

a conductive bonding layer;

a doped region of a conductivity type formed in a semiconductor substrate of a second conductivity type, wherein the doped region is underlying and surrounding the conductive

bonding layer;

a conductive region of the first conductivity type disposed in the doped region, wherein the conductive region is underlying and surrounding the conductive bonding layer and wherein the conductive region includes a surface area at least substantially equal to a surface area of the conductive bonding layer; and

a conductive tap region spaced apart from and surrounding at least a portion of the doped region, wherein a portion of the conductive tap region is electrically coupled to a supply voltage.

13. (previously presented) The bond pad of claim 12 wherein the supply voltage is a ground voltage and the conductive bonding layer includes a metal.

14. (previously presented) The bond pad of claim 12 wherein the doping concentration of the doped region is less than the doping concentration of the conductive region.

15. (previously presented) The bond pad of claim 12 wherein the conductive tap region is doped to be of an opposite conductivity type than the doped region.

16. (previously presented) The bond pad of claim 12 further including a conductive tap region portion that is spaced apart from and surrounding the doped region, wherein the conductive tap region portion is decoupled from the supply voltage to provide a predetermined resistance between the doped region and the supply voltage.

17. (previously presented) The bond pad of claim 12 wherein the conductive tap region is a continuous region.

18. (previously presented) The bond pad of claim 17 wherein the conductive tap region completely surrounds the doped region.

19. (previously presented) The bond pad of claim 12 wherein the conductive tap region is a discontinuous region.

20. (previously presented) The bond pad of claim 19 wherein the conductive tap region substantially surrounds the doped region in a concentric-like manner.

21. (previously presented) The bond pad of claim 12 wherein the conductive region is polysilicon.

22. (previously presented) The bond pad of claim 21 wherein the conductive tap region is a doped layer positioned beneath the conductive region.

23. – 38. (cancelled)